## ABSTRACT

A memory device and a method for compensating for a load current in the memory device. The memory device includes a plurality of I/O buffers where each I/O buffer includes an I/O write-buffer driver circuit. The I/O write-buffer driver circuit is coupled to a load current compensation circuit. Although each I/O buffer includes an I/O write-buffer circuit, a single load current compensation circuit may be coupled to several I/O write-buffer driver circuits. The load current compensation circuit generates a load compensation current for each I/O buffer circuit that is not being programmed. The load compensation current increases the load current so that a drain-side programming voltage (VPROG) drives a substantially constant load current, wherein the drain-side programming voltage is substantially independent of the number of bits being programmed.